RELIABLE HYSTERESIS CURRENT CONTROLLED DUAL BUCK HALF BRIDGE INVERTER

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Abstract: A highly efficient and reliable topology- dual buck half bridge inverter (DBI) is introduced. The existence of discontinuous conduction mode (DCM) operation state requires the bias of inductor current for DBI implemented with linear controllers like ramp comparison SPWM (RCSPWM) controllers. A novel operation scheme for DBI and a hysteresis current controlled dual buck half bridge inverter (HCDBI) are proposed. The bias current required by RCSPWM DBI is eliminated and conduction losses are dramatically reduced. HCDBI has greatly improved the modulation performance in DCM region for the benefit of its excellent command tracking capability. The operational scheme and control strategy are presented. Power losses of the conventional half bridge inverter (CHBI) and HCDBI are compared with mathematical computation, and experimental verification is also executed. Both calculational and experimental results verify that HCDBI has a superior switching performance over CHBI. Its excellent high frequency operational capacity provides another access to realize high frequency operation of inverters.

Key words: high frequency; switching; inverters; hysteresis current control; half bridge
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INTRODUCTION

A key issue in power electronics is attainment of high efficiency for the converter operating at high switching frequency. Soft-switching technique has demonstrated promise in obtaining high frequency operation of converters, and great efforts have been made to apply this technique to inverters. Soft-switching inverters such as resonant pole inverter[1], resonant DC link inverter[2], resonant snubber inverter[3], etc. have found successful applications in particular occasions. Whereas these solutions suffer from redundant circuit configuration and control strategy, challenge of tuning, and deteriment to the optimum modulation of output voltage waveform. There are scarcities of CONCISE soft-switching inverter techniques.

A highly reliable two-switch inverter (Fig. 1(a)) was reported in Ref. [4]. It is composed of a buck converter and a boost one. Refs. [5, 6] made their recent efforts to apply an opposed current half bridge inverter (OCHB) (Fig. 1(b)) to power amplifiers. Actually it is composed of two buck converters, which is refered as dual buck converter (DBI) in this paper. The above mentioned inverter topologies can be classified into DCDC-based inverter topologies[7~9]. The control strategy employed in Refs. [4~6] is based on linear ramp comparison SPWM (RCSPWM) control. The normal operation of RCSPWM DBI requires a bias current to ensure the filter inductor working at continuous conduction mode (CCM). In order to further reduce the power losses induced by the bias current, a novel hysteresis current controlled dual buck inverter (HCDBI) is proposed in this paper. It can work without any bias current and

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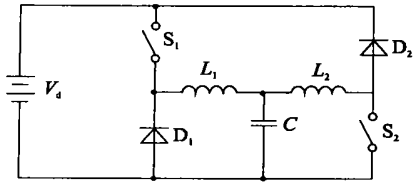
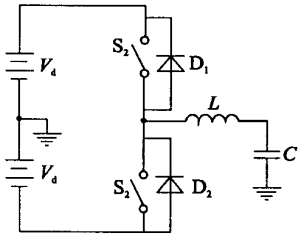
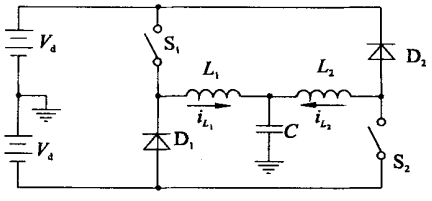
overcome the distortion problem resulting from discontinuous conduction mode (DCM) operation. Comparative study between the conventional half bridge inverter (CHBI) (Fig. 1 (b)) and HCDBI is also made. An inductor-coupled dual buck inverter (ICDBI) is also proposed and the size of the inductor is greatly reduced.



(a) Buck-boost inverter



(b) Conventional half bridge inverter



(c) Dual buck half bridge inverter

Fig. 1 Three types of inverter topologies

1 DUAL BUCK HALF BRIDGE INVERTER

The DBI main stage is composed of two simple buck converters (Fig. 1(c)). The shoot-through dI/dt is now limited by two large in-series inductors ($L_1 + L_2$). The availability of optimum design of power devices is another superior feature of DBI. For conventional bridge type inverter, when the freewheeling current moves from the body diode of the switch into another switch in the same leg, there will occur a large reverse recovery current in the non-ideal diode. This increases the switching-on loss dramatically. The novel power stage configuration of DBI mitigates the notorious reverse recovery problem naturally.

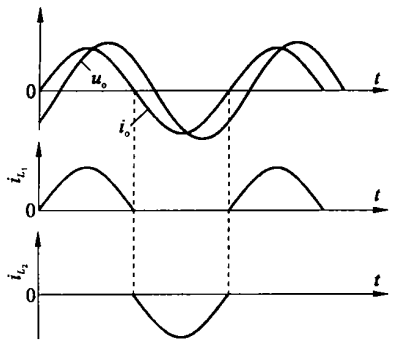
2 HYSTERESIS CURRENT CONTROLLED DUAL BUCK INVERTER

RCSPWM control is a popular linear modulation scheme. While in case of DBI, the voltage conversion ratio linearity will lose when the inductor current becomes discontinuous like the buck converter. The linear controller like RCSPWM cannot correct the output voltage distortion in DCM operation, unless it is equipped with a large filter inductor at high switching frequency. A practical solution is biasing the inductor to keep the inverter operating at CCM. But considerable conduction losses in the switches and inductors exist, which is not desirable. The DC component in load voltage also appears and it requires laborious design for elimination.

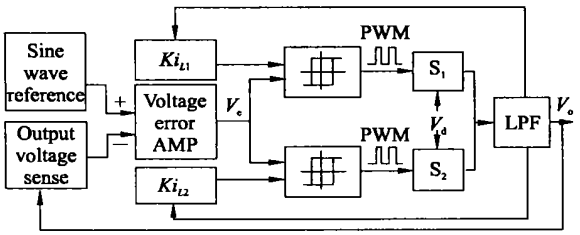
This paper proposes a novel operation scheme and current control strategy for DBI. The basic operation scheme is that two single buck converters operate alternatively in each half of the load period. The key current waveforms of two inductors are shown in Fig. 2(a). No bias current presents in the inverter. Thus excessive power losses and DC component problems induced by the bias current do not exist.

The proposed core modulator is shown in Fig. 2(b) with an inner current loop and an outer voltage loop. The filter inductor currents are fed back and the voltage error output of the ampifier V_e commands the two inductor currents alternatively in each half of the load period by two hysteresis controllers. When inductor currents approach zero, the hysteresis modulator adaptively changes the switching frequency to limit the high frequency current ripple in the referred tolerance band. The resultant DCM

region is dramatically reduced and its modulation performance in DCM is greatly improved. Low load voltage distortion is guaranteed.



(a) Key inductor current waveform



(b) Core control scheme of HCDBI

Fig. 2 Key inductor current waveform of the control scheme and core modulator

The hysteresis controller exhibits perfect command tracking up to the bandwidth limit of the voltage modulator. It also has the advantages of robustness and high gain of voltage error amplifier, which benefits the instantaneous tight regulation of output voltage.

3 INDUCTOR COUPLED DUAL BUCK INVERTER

Compared with CHBI, the obvious defect seems to be that two filter inductors are needed. Each of them leaves unused in half load period. An inductor coupled dual buck half bridge inverter (ICDBI) is proposed (Fig. 3(a)). The two filter inductors are coupled in one core and the size of the inductors is minimized. When the control strategy proposed in Section 2 is implemented, the high operation reliability feature never loses. L_1 and L_2 are the parasitic inductors of the transformer or the added discrete inductors, whose inductance has the same value L.

When S_1 is working and no currents flow through winding N_2, L_2, S_2 and D_2, winding N_1 can be looked upon as an inductor L_{m1} whose value is L_m. The voltage across L_{m1} is

$$V_1 = (V_d - V_o)\frac{L_m}{L + L_m} \tag{1}$$

Optimum coupling of L_{m1} and L_{m2} is assumed, so we have

$$V_1 = -V_2 \tag{2}$$

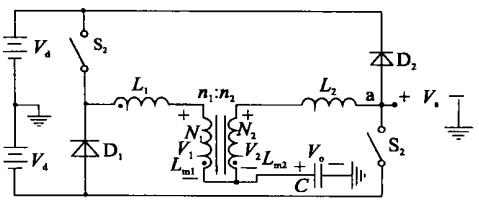
The voltage V_a of point a to neutral point is

$$V_a = V_o + V_2 \tag{3}$$

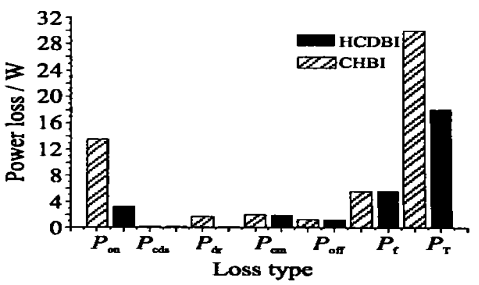
Based on Eqs. (1~3), expression of V_a is derived

$$V_a = V_o + \frac{L_m}{L + L_m}(V_d - V_o) = \left(1 - \frac{L_m}{L + L_m}\right)V_o + \frac{L_m}{L + L_m}V_d \tag{4}$$

Obviously, V_a is lower than V_d. Thus no excessive voltage stress is imposed on S_2(S_1). In addition, D_2 (D_1) will not be forced to be conducted when S_1(S_2) and D_1(D_2) are working. This is the result of theoretical analysis, and experimental study is to be conducted.



(a) ICDBI topology



(b) Comparison of power losses of HCDBI and CHBI

Fig. 3 Inductor-coupled dual buck half bridge inverter and comparison of power losses of HCDBI and CHBI

4 COMPUTATION OF INVERTER POWER LOSSES

In this paper, the switching loss is the most concerned and core loss is not included. The total involved power loss of the inverter is

$$P_T = P_{on} + P_{off} + P_{cds} + P_{dr} + P_f + P_{cm} \quad (5)$$

where P_{on}, P_{off}, P_{cds}, P_{dr}, P_f, P_{cm} are given in Table 1.

The switching loss computation of the hysteresis current controlled inverter is the most challenge for that the switching frequency is variable over one load cycle. An assumption is made that the switching frequency is constant and is equal to the average switching frequency.

The switching-on losses of the switches consist of two main parts. One part (P_{ds}) is due to the discharging of drain to source parasitical capacitor C_{ds} in every switching action, and the other part (P_{on}) is the commutation loss due to the overlap of switching voltage and current. P_{ds}, P_{on}, the switch conduction loss P_{cm}, the switching-off loss P_{off}, the switching-off loss of diodes P_{dr}, and the filter inductor's conduction loss P_f are all given in Table 1.

Table 1 Derived expressions of different types of power losses

P_{cds}	P_{on}	P_{off}	P_{dr}	P_{cm}	P_f
$\frac{1}{2}C_{ds}V_d^2F_s$	$2F_oV_dT_{on}\sum_{k=1}^{\frac{1}{4F_s}}(i_{Lk}+I_{rr})$	$2F_oV_dT_{off}\sum_{k=1}^{\frac{1}{4F_s}}(i_{Lk})$	$V_dQ_{rr}F_s$	$I_f^2R_{ds}$	$I_f^2R_f$

Here V_d, I_f, F_s, F_o, R_f, T_{on}, T_{off} and R_{ds} signify DC input voltage, rms value of inductor current, average switching frequency, load frequency, filter inductor resistance, and switching-on time, switching-off time, on-resistance of the switch, respectively. And $i_{Lk}(k = 1, 2, \cdots)$ represent the inductor current value at the instant the switch turns on for the kth time $\left(i_{Lk} = I_f\sin\frac{2k\pi F_o}{F_s}\right)$.

Power loss calculations of CHBI and HCDBI are made based on the obtained expressions above. The results of power loss distribution and comparison are illustrated in Fig. 3(b). The Figure shows that HCDBI exhibits the prevailing switching performance over CHBI. This superior feature of high frequency operation capacity allows HCDBI to exhibit the excellent performance to supply nonlinear load for its small filter inductor, great system robustness, high gain of voltage error amplifier, wide system bandwidth and tight instantaneous regulation of the output voltage. The tested result of HCDBI supplying nonlinear load for verification is shown in Section 5.

5 EXPERIMENTAL RESULTS

Experimental prototypes of CHBI and HCDBI are built to verify the operation performance of the proposed control strategy. Both inverters adopt two stage DC-DC-AC configurations and each has the same DC-DC pre-regulator. The input voltage range is 18～32 V and the output is 21 V_{rms}/340 V_A/400 Hz. The inverters are operating at two groups of parameters (A, B) listed in Table 2. MOSFET FQA140N10 and diode MUR3020 are used.

Table 2 Two groups of operational parameters of HCDBI and CHBI

	A			B		
	$L(L_2, L_1)/\mu H$	$C/\mu F$	F_s/kHz	$L(L_2, L_1)/\mu H$	$C/\mu F$	F_s/kHz
HCDBI	54	50	30	34	50	40
CHBI	54	50	30	34	50	35

The tested efficiencies are obtained at 28.5 volts input and resistive load condition (Fig. 4). The Figure shows that HCDBI has 86% efficiency at full load, with 3% improvement over CHBI. When the filter inductor is reduced from 54 μH to 34 μH, HCDBI operating at 40 kHz is only 1% lower in efficiency than HCDBI operating at parameters *A* under full load, while exhibiting 2% higher than CHBI operating at 35 kHz. The filter capacitor is to be diminished for optimization when operating at higher frequency. The DC component of the load voltage is lower than 0.01 V.

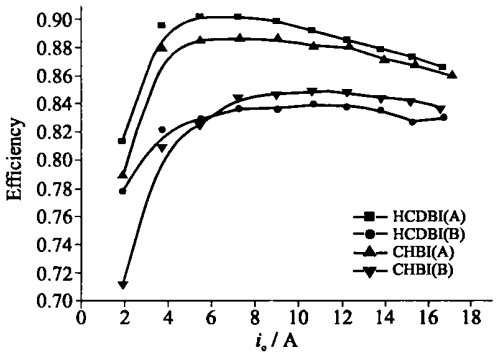
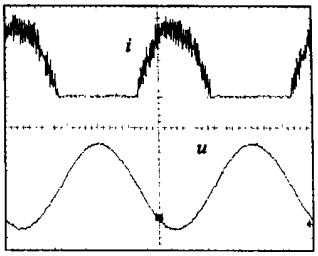


Fig. 4 Tested efficiencies of HCDBI and CHBI operating at two groups of parameters under resistive load

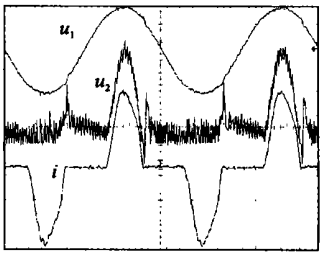
Fig. 5 shows waveforms of filter inductor current and load voltage of HCDBI at full resistive load. The Figure shows that HCDBI presents minimum distortion in DCM operation intervals and produces nearly perfect sinusoidal voltage (THD ≯ 0.7%). A test has been conducted connecting a rectifier with a capacitive filter to the inverter. Fig. 6 shows waveforms of voltage signal of the sensed current of one filter inductor (u_2), load current (i) and output voltage (u_1) of HCDBI under full capacitive rectifier load (P_o = 340 W). The measured THD of the output voltage is only 3%.

Fig. 5 shows one filter inductor current "i" and load voltage "u" of HCDBI at full resistive load. Fig. 6 shows sensed voltage signal "u_2" of the current of one filter inductor, load current "i" and output voltage "u_1" of HCDBI under full capacitive rectifier load: P_o = 340 W, C_{rect} = 18 800 μF (C_{rect} is the filter capacitor directly behind the rectifier bridge), L_1 = L_2 = 34 μH, C = 50 μF.



u: 20 V/div, i: 10 A/div, t: 500 μs/div

Fig. 5 Current (i) and voltage (u) waveforms of HCDBI



u_1: 20 V/div, u_2: 2 V/div, i: 10 A/div

Fig. 6 u_1, u_2 and i waveforms of HCDBI

6 CONCLUSION

A novel operation scheme and hysteresis current control strategy for DBI has been proposed in this paper. HCDBI is capable of producing nearly perfect sinusoidal voltage without any bias current. Both computation and experimental results verify the superior switching performance of HCDBI over CHBI. This allows it to operate at high frequency with small filter inductor and possess wide system bandwidth. Excellent capability to supply nonlinear load is also obtained.

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一种可靠的滞环电流型双降压式半桥逆变电路

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摘要: 研究了一种新颖的双降压式半桥逆变电路(Dual buck half bridge inverter, DBI), 该电路有无直通, 效率高等特点。提出了一种 DBI 的无偏置电流运行方式和一种滞环电流型双降压式半桥逆变电路(Hysteresis current controlled dual buck half bridge inverter, HCDBI), 消除了采用载波交截 SPWM 控制 DBI 正常工作所必需的偏置电流, 进一步提高了效率。对 HCDBI 和传统半桥逆变器进行了理论上的损耗计算分析和实验验证, 证明了 HCBBI 可大幅降低开关损耗, 开关频率高, 滤波器小。为实现逆变器的高频化提供了一种简洁的方法和新的途径。

关键词: 高频; 开关; 逆变器; 滞环电流控制; 半桥

中图分类号: TM 464